## REMARKS

This is in response to the Office Action dated June 2, 2005.

Claim 35 stands rejected under 35 U.S.C. Section 112, first paragraph, in sections 3-4 of the Office Action. In this respect, claim 35 has been amended to recite that the *scanning line* and storage capacitor electrode are fabricated from a same material in a single patterning. Thus, this Section 112 issue has been addressed and resolved.

Claim 12 stands rejected under 35 U.S.C. Section 112, second paragraph, in sections 5-6 of the Office Action. Claim 12 has been amended to clarify that the signal line and scanning line are not formed in the same patterning at the same time as requested by the Examiner. Thus, this Section 112 issue has been addressed and resolved.

Claim 9 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Jung Mok. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 9 requires "*a storage capacitor common wire disposed parallel to the signal line*." For example, and without limitation, Fig. 24 of the instant application illustrates storage capacitor common wire 14 disposed parallel to signal line 11. This feature is advantageous, for example and without limitation, in that a lower time constant of the signal lines may be realized. In particular, for example and without limitation, the instant specification on page 20, lines 8-16, describes the advantageous effect of realizing a relatively low time constant of the signal lines, which is derived from the electrostatic capacity between the signal lines and the other wires that is reduced by the signal lines crossing none of the storage capacitor common wires in a central area of the device; see also page 73, line 24 to page 74, line 9.

The Fig. 4-6 embodiment of Jung Mok fails to disclose or suggest the aforesaid underlined feature of claim 9. Instead, in the Fig. 4-6 embodiment of Jung Mok, the capacitor common wiring 81b is parallel to the scanning line 60 – not to the signal line 70. In other words, in the Fig. 4-6 embodiment of Jung Mok the capacitor common wiring 81b is *perpendicular* to the signal (source) line 70; not "*parallel*" to it as claim 9 requires. Thus, not only does Jung Mok fail to disclose or suggest the invention of claim 9, but it teaches directly away from the same.

Additionally, Jung Mok also fails to disclose or suggest a storage capacitor electrode and a storage capacitor common wire *being patterned in different steps so as to have an insulation film provided partially therebetween* as required by claim 9. In Jung Mok, 81b is both the storage capacitor electrode and the wiring therefore; and thus the two are formed at the same time which is the opposite of what claim 9 requires. Moreover, one of ordinary skill in the art would readily recognize that transparent pixel electrode 91 cannot be considered a "storage capacitor common wire" as alleged in the Office Action (it is also noted that 91 cannot be considered "parallel" to the signal line).

Claim 12 requires the "*storage capacitor common wire disposed at least partially parallel to the signal line.*" Jung Mok fails to disclose or suggest this. Jung Mok also fails to disclose or suggest the subject matter recited in the last paragraph of claim 12.

Claim 14 requires the "storage capacitor common wire disposed at least partially parallel to the signal line." As explained above with respect to claim 9, Jung Mok fails to disclose or suggest this. Citation to Oh cannot cure this flaw in the base reference Jung Mok.

Claim 35 requires the "*storage capacitor common wire disposed at least partially parallel to the signal line.*" Again, Jung Mok fails to disclose or suggest this. Citation to Jeromin cannot cure this flaw in the base reference Jung Mok. Still further, Jung Mok also fails

to disclose or suggest the storage capacitor electrode and storage capacitor common wire being patterned in different steps so as to have an insulating film provided partially therebetween as required by claim 35.

Claim 42 requires the "*storage capacitor common wire disposed parallel to the signal line.*" As explained above, Jung Mok fails to disclose or suggest this. Jung Mok also fails to disclose or suggest the signal line and the pixel electrode being fabricated from a single conductive layer through patterning thereof as called for in claim 42.

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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